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10/079,057	02/19/2002	Eric R. Garlepp	SILA:107	5951
7590 04/22/2005			EXAMINER	
O'KEEFE, EGAN & PETERMAN, L.L.P.			PHU, SANH D	
Building C, Suite 200 1101 Capital of Texas Highway South Austin, TX 78746			ART UNIT	PAPER NUMBER
			2682	
			DATE MAILED: 04/22/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/079,057	GARLEPP ET AL.				
Office Action Summary	Examiner	Art Unit				
	Sanh D Phu	2682				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply If NO period for reply is specified above, the maximum statutory period of Failure to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be tim within the statutory minimum of thirty (30) day will apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
1)⊠ Responsive to communication(s) filed on <u>08 Fe</u>	ebruary 2005.					
<u>_</u>	action is non-final.					
•	, <del></del>					
Disposition of Claims						
4) ☐ Claim(s) 1 and 4-74 is/are pending in the appli 4a) Of the above claim(s) is/are withdray 5) ☐ Claim(s) is/are allowed.  6) ☐ Claim(s) 1 and 4-74 is/are rejected.  7) ☐ Claim(s) is/are objected to.  8) ☐ Claim(s) are subject to restriction and/o	vn from consideration.					
Application Papers						
9) The specification is objected to by the Examine						
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
Applicant may not request that any objection to the	• • • • • • • • • • • • • • • • • • • •					
Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Ex						
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:  1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority application from the International Bureau * See the attached detailed Office action for a list	s have been received. s have been received in Applicati rity documents have been receive u (PCT Rule 17.2(a)).	on No ed in this National Stage				
Attachment(s)	_					
1) Notice of References Cited (PTO-892)	4) Interview Summary Paper No(s)/Mail D					
<ol> <li>Notice of Draftsperson's Patent Drawing Review (PTO-948)</li> <li>Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date</li> </ol>		Patent Application (PTO-152)				

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#### **DETAILED ACTION**

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1. This Office Action is responsive to the Amendment filed on 2/8/05.

### Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35
U.S.C. 102 that form the basis for the rejections under this section made in this
Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 3. Claims 1, 35-37 and 63-65 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsumura (5,883,553), previously cited.

As per claims 1, 35, 36, 37, 63, 64, see figures 3 and 7, and col. 3, line 58 to col. 5, line 12, col. 6, line 19 to col. 10, line 5, Tsumura discloses a method and associated system (figure 7) comprising:

a filter circuitry (21, 22) with an output (outputted from element (21) or (22)) (see figure 3), having an output impedance, the filter filtering signals outside a signal band of interest, wherein the filter circuitry can be

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implemented to receive and filter a radio frequency in a MHz range (see col. 1, lines 51-56); and

an impedance matching network (31, 32) (see figure 3), with an input coupled to the output of the filter circuitry, the impedance matching network further having an output (106) (see figure 3) coupled to a signal processing circuitry (52) having an input impedance, wherein the impedance matching network matches the input impedance of the signal processing circuitry to the output of the filter circuitry (see col. 9, line 18 to col. 10, line 4).

As per claim 65, Tsumura discloses that the filter circuitry can be implemented to receive and output rf signals in a MHz range for further processing (see col. 1, lines 51–56).

# Claim Rejections - 35 USC § 103

- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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5. Claims 4, 5, 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura in view of Broderick (5,170,500), previously cited.

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As per claims 4, 5 and 66, Tsumura does not disclose whether the signal processing circuitry comprises an amplifier.

Tsumura discloses that the signal processing circuitry performs a frequency conversion. However, he does not disclose how the frequency conversion is implemented.

Broderick a frequency conversion (31, 32, 33) comprising an amplifier (31) at its receive front end receiving its input signal (see figure 2, and col. 4, line 38-58).

Therefore, for an application, it would have been obvious for one skilled in the art, when building Tsumura invention, to implement the signal processing circuitry to perform a frequency conversion comprising an amplifier, as taught by Broderick, since Tsumura does not teach how its required frequency conversion is implemented in-detail.

6. Claims 6-31, 67-70, 72-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura in view of Broderick, and further in view of Keane et al (5,195,045), previously cited.

As per claims 6, 11, 14, 18, 21, 26, 29, 67, 68, 69, 70, 72, 73, Tsumura, in view of Broderick, does not disclose the impedance matching network comprising a L-network,  $\pi$ - network, T-network, or a plurality of L-networks,  $\pi$ - networks or T-networks.

Tsumura, in view of Broderick, does not disclose how the impedance network is implemented.

Implementing an impedance network as a L-network/ $\pi$ - network/T-network is well-known in the art. For instance, Broderick teaches that an impedance matching network can be implemented as a L-network/ $\pi$ -network/T-network (see col. 1, lines 55-58).

Therefore, for an application, it would have been obvious for one skilled in the art, when building Tsumura invention, in view of Broderick, to implement impedance matching network (31, 32) with a L-network/ $\pi$ - network/T- network for element (31), as taught by Keane et al., and another L-network/ $\pi$ -

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network/T-network for element (32), as taught by Keane et al, to maximize the output power transfer from the filter circuitry to the signal processing circuitry since Tsumura, in view of Broderick, does not disclose how the impedance network is implemented in detail.

As per claims 7, 8, 12, 13, 15, 16, 19, 20, 22, 23, 27, 28, 30, 31, Tsumura discloses that the signal processing circuitry comprises an output (303) (see figure 7).

As per claims 9, 10, 17, 24, 25, Tsumura, in view of Broderick and Keane et al, teaches that the impedance network comprises inductors and capacitors (see Keane et al, see col. 1, lines 55-58).

Claim 74 is is rejected with similar reasons set forth for claim 42.

7. Claims 32-34, 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura in view of Broderick, and further in view of Kodulkula (6,177, 872), previously cited.

As per claim 32, 71, Tsumura, in view of Broderick, does not disclose the impedance matching network comprising a transmission line.

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Tsumura, in view of Broderick, does not disclose how the impedance network is implemented.

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Implementing an impedance network as a transmission line network is well-known in the art. For instance, Kodulkula teaches that an impedance matching network can be implemented as a transmission line network (102) (see figure 1, and col. 3, line 54 to col. 4, line 35).

Therefore, for an application, it would have been obvious for one skilled in the art, when building Tsumura invention, in view of Broderick, to implement impedance matching network (31, 32) with a transmission line network for element (31), as taught by Kodulkula, and another transmission line network for element (32), as taught by Kodulkula, to maximize the output power transfer from the filter circuitry to the signal processing circuitry since

Tsumura, in view of Broderick, does not disclose how the impedance network is implemented in detail.

Claims 33 and 34 are rejected with similar reasons set forth for claims 7, 8, 12, 13, 15, 16, 19, 20, 22, 23, 27, 28, 30, 31.

8. Claims 38, 43, 48, 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura in view of Keane et al.

Claim 38 is rejected with similar reasons set forth for claims 6 and 11.

Claim 43 is rejected with similar reasons set forth for claims 14 and 18.

Claim 48 is rejected with similar reasons set forth for claims 21 and 26.

Claim 53 is rejected with similar reasons set forth for claim 29.

9. Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura, in view of Kodulkula.

Claim 58 is rejected with similar reasons set forth for claim 32.

10. Claims 39-42, 44-47, 49-52, 54-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura, in view of Keane et al, and further in view of Broderick.

Claims 39-41 are rejected with similar reasons set forth for claims 6 and 11.

As per claim 42, in Tsumura, in view of Keane et al and Broderick, an second integrated circuit(s) following the frequency conversion section (52) (see Tsumura, figure 7) is inherently included for receiving the output signal

outputted from port (303) for further processing. Tsumura, in view of Broderick and Keane et al does not disclose that frequency conversion section (52) outputs a digital output signal at port (303). However, implementing circuitry as a digital circuit, analog circuit or a combination of them is well-known in the art, and the examiner takes Official Notice. Therefore, it would have been obvious for one skilled in the art, within his skills and based on his design preference, to implement frequency conversion section such that the element (32) (see Broderick, figure 2) as a digital circuit for outputting the output signal at port (303) as a digital signal.

Claims 44-46 are rejected with similar reasons set forth for claims 14 and 18.

Claim 47 is rejected with similar reasons set forth for claim 42.

Claims 49-51 are rejected with similar reasons set forth for claims 21 and 26.

Claim 52 is rejected with similar reasons set forth for claim 42.

Claims 54-56 are rejected with similar reasons set forth for claim 29.

Claim 57 is rejected with similar reasons set forth for claim 42.

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11. Claims 59-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura, in view of Kodulkula, and further in view of Broderick.

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Claim 59-61 are rejected with similar reasons set forth for claim 32.

Claim 62 is rejected with similar reasons set forth for claim 42.

### Response to Arguments

12. Applicant's arguments filed on 2/8/05 have been fully considered but they are not persuasive.

The applicant mainly argues that (i) with respect to claims 1, 35, 63,

Tsumura does not disclose the filter output (outputted from filter (21) (see figure 3)) as being a differential output, the impedance matching network input (inputted to impedance matching network (31)) as being a differential input, and the impedance matching network output (outputted from impedance matching network (31)) as being a differential output; and (ii) Tsumura does not disclose that the filter (21) receives radio input signal and provides a radio output signal.

Regarding to part (i), the examiner respectfully disagrees. Tsumura discloses that the filter (21) is a conventional filter being implemented with

passive elements (see col. 1, lines 18-23 and col. 4, lines 16-19). Such a conventional filter inherently comprises the input as a differential input, which includes two input ports connected to two lines for receiving an input signal and its return signal for filtering said input signal, and the output as a differential output, which includes two output ports connected two lines for outputting the filtered signal and obtaining its return signal. In order to clarify this matter, the examiner now cites Woff et al, "Microwave Engineering and System Application" teaching such a conventional filter (see figure 9.7, and page 242). Therefore, Tsumura filter output (outputted from filter (21) (see figure 3)) is inherently a differential output. Further, since in Tsumura, the impedance matching network (31) has its input being coupled to said filter at said filter's output in order to impedance-match said filter output with a further processing stage (see figure 3 and col. 4, lines 28-48), the impedance matching network input, therefore, must also be a differential input in order to be coupled with said filter output (being a differential output, as explained above), and the impedance matching network output must, therefore, be also a differential output in order to correspond with said impedance matching

network's differential input. For clarifying the features of such a matching network, the examiner now cites Keane et al. (prior art of record) teaching a matching network (220a) comprising matching network differential input (222a, 223a) coupled with differential output (44, 45) of device (40) and matching network differential output (224a, 225b) coupled with a further processing stage (2300) to match said device (40) with said further processing stage (see figure 1 and 2A and col. 6, line 55 to col. 7, line 60).

Regarding to part (ii), the examiner also disagrees, Tsumura discloses that the filter (21), with filter bandwidth (d1) having center frequency (f1), can be implemented to receive a radio signal in a MHz range, as its radio input signal for filtering said radio signal and to provide the filtered radio signal as its radio output signal (see col. 1, line 51 to col. 2, line 5, and col. 3 line 66 to col. 4, line 20, col. 6, lines 19–51).

Based on the above rationale, it is believed that the limitations of claims are still met and therefore, the rejections are still maintained.

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#### Conclusion

13. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sanh D Phu whose telephone number is (703)305-8635. The examiner can normally be reached on 8:00-16:30.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sanh D. Phu Examiner Art Unit 2682

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